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PATENT APPLICATION OF

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FOR

STACKED MODULATOR AND AUTOMATIC GAIN CONTROL AMPLIFIER

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STACKED MODULATOR AND AUTOMATIC GAIN CONTROL AMPLIFIER

Technical Field

The present invention relates to a circuit arrangement in which a modulator and an automatic gain control (AGC) amplifier are connected to each other so as to avoid unnecessary signal transformation and to re-use the modulator current in the AGC so as to save power.

Background of the Invention:

It is known in the art to have a circuit arrangement for combining two circuits so as to use a common supply voltage. Thus it is known such as in EP 0 442,637 to combine a high frequency amplifier circuit with a filter circuit such that the radio frequency amplifier circuit serves as a filter for the supply voltage produced by the supply voltage of the amplifier. Such a circuit arrangement can overcome the shortcomings of having a separate amplifier and filter circuit since the circuit arrangement uses current passing through the amplifier transistor for two purposes; namely, in conjunction with amplifying the input signal of the amplifier and for purposes of supplying current for the supply voltage to be produced. With respect to automatic gain control amplifiers, it is not known to combine such an amplifier for gain/power control in combination with a modulator so as to effectively stack the stages and thereby use the modulator current for the automatic gain control amplifier as well.

Summary of the Invention:

The present invention provides for use of a common supply current from the modulator for both an automatic gain control amplifier and the modulator associated with modulation of input signals by a local oscillator reference signal. Such an architecture is particularly suitable for use in NMP's current GSM transmitters used in the wireless industry. It is particularly suited for GSM-EDGE systems which, due to the requirements of such systems, present new challenges in transmitter design, one of them being a very tight Error Vector Magnitude (EVM). In order to meet this

requirement, the power amplifier must be more linear than those used in prior GSM transmitters. One solution for this greater linearity requirement is to remove the gain control from the power amplifier and to use a linear amplifier instead. The gain control must then be performed in a separate gain control stage.

The present invention is particularly directed to use of a separate automatic gain control (AGC) amplifier stage that can be stacked with the modulator of the transmitter. The circuit topology presented herein enables a combination or "stacking" of the automatic gain control and the amplifier modulator. The modulator is a Gilbert cell-type double balanced structure and the AGC amplifier is based upon a current steering methodology. With this design, a very low voltage direct conversion modulator and an AGC amplifier can be stacked that enables re-use of the modulator current in the AGC amplifier. The circuitry is particularly designed for integration into a wireless telephone radio frequency integrated circuit (RFIC).

Brief Description of the Drawings:

For a fuller understanding and nature and objects of the present invention, reference should be made to the following detail description, taken in conjunction with the following drawings in which:

Figure 1 is an overall block diagram of a prior art GSM transmitter;

Figure 2 is a block diagram of a GSM-EDGE transmitter necessary for obtaining better power amplification linearity than that used in a prior art GSM transmitter;

Figure 3 is a block diagram of a typical GSM-EDGE type transmitter incorporating a stacked modulator and automatic gain control (AGC) amplifier according to the present invention;

Figure 4 is a schematic diagram of a stacked modulator (balanced design) and automatic gain control amplifier according to the present invention;

Figure 5 is a schematic diagram of a stacked modulator and automatic gain control amplifier similar to that shown in Figure 4 with the other half of the modulator the same as the half shown (balanced structure), further incorporating a non-inverting gain stage;

Figure 6 is a schematic diagram of a stacked modulator and automatic gain control amplifier similar to that shown in Figure 4 with the other half of the modulator the same as the half shown (balanced structure), further incorporating an inverting gain stage;

Figure 7 is a schematic diagram of a stacked modulator and automatic gain control amplifier similar to that shown in Figure 4 with the other half of the modulator the same as the half shown (balanced structure), further incorporating an inverting gain stage with common mode feedback;

Figure 8 is a schematic diagram of a stacked modulator and automatic gain control amplifier similar to that shown in Figure 4 with the other half of the modulator the same as the half shown (balanced structure), further incorporating a current mode input signal from a digital/analog converter that is converted to a voltage with reference resistors;

Figure 9 is a schematic diagram of a stacked modulator and automatic gain control amplifier similar to that shown in Figure 4 with the other half of the modulator the same as the half shown (balanced structure), further incorporating a low frequency filter and a noise filter;

Figure 10 is a schematic diagram of a stacked modulator and automatic gain control amplifier similar to that shown in Figure 4 with the other half of the modulator the same as the half shown (balanced structure), further incorporating a noise filter and a parallel input stage without associated low frequency reference signals being used with the parallel input stage.

Best Mode for Carrying Out the Invention:

Figure 1 is a block diagram of a wireless GSM transmitter having a direct conversion architecture. The analog components of the GSM transmitter are the digital/analog converter **20**, a filter **22**, a modulator **24**, a transformer (balun) **26**, and

a power amplifier **28** having an automatic gain control amplifier incorporated therein. A transformer **26** is used to convert the differential output of the modulator into a single-ended signal **27** for use by a typical power amplifier **28**. Such power amplifiers usually have a single-ended input. For next generation GSM-EDGE systems, there are new challenges placed on the transmitter design, one of them being the requirement for a very tight Error Vector Magnitude (EVM). In order to meet this requirement, the power amplifier must be implemented so as to have a much more linear gain than that used in a standard GSM transmitter. One solution which has been suggested is to remove the gain control from the power amplifier and to present the gain control as a separate gain control stage. In this manner, the power amplifier can be designed to have a more linear gain over its operating frequency. Figure 2 represents such design in which the components are the same as shown in Figure 1, except that a separate automatic gain control amplifier **30** is presented between the modulator **24** and the transformer **32** and a separate linear power amplifier **34** is used in place of the power amplifier with an integrated AGC as shown in Figure 1.

The circuit arrangement shown in Figure 2, although acceptable, does present added circuit design requirements to the radio frequency integrated circuit (RFIC) typically used in wireless devices. The overall block diagram of a typical transmitter for a GMS-EDGE system incorporating the technology of the present invention is shown in Figure 3. As there seen, the modulator **24** and the automatic gain control (AGC) amplifier **30** are stacked relative to each other in a circuit arrangement **36**. The modulator and AGC amplifier stages are therefore arranged in such a manner that the modulator current is re-used in the AGC amplifier, thereby resulting in associated current savings. This arrangement also eliminates unnecessary signal transformation from a current signal to a voltage signal between the modulator and the AGC amplifier. Furthermore, this arrangement provides that the input stage of the modulator can be very linear through use of operational amplifiers with associated feedback. The input stage associated with this circuit is more involved than prior art modulators which use a PMOS transistor and a current mirror rather than the present invention's use of operational amplifiers. Furthermore, a very low voltage supply Vcc can be used for a direct conversion modulator thereby achieving a 1.4 volt peak-to-peak linear output at the output of the automatic gain control circuit with use of a 2.5

volt Vcc power supply. The 1.4 volt peak-to-peak signal represents a +10dBm power gain into a 100 ohm load.

Embodiments of the Invention:

As best seen in Figures 3 and 4 (comprising Figures 4A and 4B) the circuit arrangement **36** comprises modulator **24** and stacked automatic gain control (AGC) amplifier **30**. Throughout the description it should be noted that the modulator forming part of this circuit arrangement uses a balanced structure comprising inband and quadrature portions and thus the signal inputs and local oscillator inputs have both inband and quadrature portions. Inband signals and associated components are designated with an "_I" suffix and quadrature signals and components are designated with an "_Q" suffix. Only Figure 4 shows both the inband and quadrature portions of the circuitry and it is understood that the other figures have such portions, but only the inband portion is shown. In this description, reference to a signal or component is made to the combination of both the inband and quadrature portions. For instance, reference to signal inputs IN+ and IN- means reference to inband signals inputs IN+_I and IN-_I as well as quadrature signal inputs IN_Q and IN-_Q. As shown in Figure 4, modulator **24** has an inband portion **24_I** and a quadrature portion **24_Q**.

The modulator **24** and the automatic gain control (AGC) amplifier **30** are stacked relative to each other so that the AGC amplifier is able to re-use the modulator current at the modulator outputs **40** and **41**. The signal inputs (IN+ and IN-) are presented to the modulator at a pair of inputs **38**, **39** of operational amplifiers OP1 and OP2 with the other input terminal of the operational amplifiers (inputs of opposite polarity) respectively connected to resistors R3 and R4. The outputs **44** and **45** of the operational amplifiers represent a transformation of the input voltage to a current. The current presented at operational amplifier outputs **44** and **45** is converted to a modulated output at outputs **40** and **41** of modulating circuit **47** and **48** represented by transistors Q1, Q2, capacitors C1, C2 and resistors R5, R6 for modulator circuit **47** and transistors Q3, Q4, capacitors R7 and R8 and for modulator circuit **48**. The modulation signal is obtained from a local oscillator reference signal presented at inputs LO+ and LO-. This modulation signal can be an intermediate frequency (IF)

or a direct conversion modulation signal. For wireless applications this local oscillator modulation signal can therefore vary from approximately 100 MHz to 5.4 GHz.

It should be noted that the AGC amplifier **30** receives the modulated output at outputs **40** and **41** of modulator **24**. The current signal is gain controlled by the AGC amplifier **30** through use of transistors Q5, Q6, Q7 and Q8. Transistor pairs Q5/Q6 and Q7/Q8 form two current steering pairs. Both the inband and quadrature outputs **40**, **41** connect to these transistor pairs. The modulator is therefore a double balanced quadrature modulator. The amount of power presented to load R1 and R2 (with associated inductors L1 and L2) and to output terminals OUT+, OUT- is regulated by the voltage presented across inputs VM, VP. Since the signal current (modulated current signal at outputs **40**, **41**) are in opposite phase, power that is not presented at OUT+, OUT-, is presented to the other half of the AGC amplifier outputs. Thus, the AGC amplifier "dumps" part of the modulator current (and therefore power) to Vcc. It should be noted that the output power (current) of the modulator is constant and that the output power of the AGC amplifier is equal to or less than the modulator output power. This circuit arrangement does not imply low efficiency since high output power (>0 dBm) at the modulator output is required in any case (signal to noise (S/N) ratio must be very high). This circuit arrangement therefore enables re-use of the large current generated by the modulator.

Although outputs OUT+, OUT- shown in Figure 4A are directly connected to R1, L1 and R2, L2 respectively, it would be known to a person of ordinary skill in the art that a capacitor or a capacitor in series with an inductor could be placed between R1, L1 and OUT+ and between R2, L2 and OUT-.

Figures 5, 6, 7 and 8 represent various modifications which can be made to the basic invention presented in Figure 4. As seen in Figure 4, the circuitry shown represents one-half of the entire circuitry, with the circuit topology being balanced. Thus in Figure 5 a non-inverting gain stage **50** is shown which receives the signal inputs IN+, IN-, as well as a voltage reference VREF. These signals are presented to the operation amplifiers OP1 and OP2 in conjunction with feedback resistors. It should be noted that in these embodiments there is no feedback from the modulator that can lower the linearity of the AGC amplifier.

Figure 6 represents a modification of the basic circuit in which an inverting gain stage **52** is used in conjunction with receipt of the signal inputs IN+, IN- with the voltage reference VREF (note that the signal inputs effectively connect to the negative inputs of the operational amplifiers). As noted above, the constant modulator current is re-used in the AGC amplifier although the AGC amplifier output current is equal to or less than the modulator output current. This circuit arrangement does not imply low efficiency for the reasons presented above.

Figure 7 shows the use of an inverting gain stage **54**, further having a common mode feedback. The input signals IN+, IN- are presented to the common mode feedback amplifier CMFB with the associated feedback resistors. The common mode feedback helps minimize the effects of the base to emitter voltage temperature variation associated with the bipolar junction transistor (BJT) modulator transistors Q1, Q2, Q3 and Q4 due to the output power changes.

Figure 8 is another embodiment of the present invention which incorporates input stages **56** and **58** so as to compensate for lot variation of emitter resistors R3 and R4 by compensating with a current mode input signal from the digital-to-analog converter that is converted to a voltage by use of reference resistors R_{ref1} and R_{ref2}. Resistors R3, R4, R_{ref1} and R_{ref2} have the same lot variation.

Figure 9 is another embodiment of the present invention, further comprising an RF filter **60** (RF filtering) as well as a noise filter **62** (NOISE FILTERING) associated with the operational amplifiers OP1 and OP2.

Finally, Figure 10 is a further embodiment of the present invention having the noise filtering shown in Figure 9 but further having a parallel input stage local oscillator signal circuit **64**. The parallel input stage without the local oscillator signal is able to eliminate the needs for further noise filtering associated with the parallel input stage. Furthermore, when resistors R3b...R8b are ten times larger than R3a...R8a and the transistor Q5...Q8 are ten times smaller in area than transistors Q1...Q4, the overall current consumption only increases by approximately ten percent. The reason for this result can best be understood with reference to Figure 9. It is there seen that there are eight total RC filters (four shown, balanced structure). Four filters are used for noise filtering and four are used to filter out the local oscillator signal from the feedback paths. Since the -3 dBm low pass corner frequency of each

filter must be low in GSM applications (approximately 500 kHz) the RC product (resistance times capacitance) must be large. Large RC products therefore require large resistor values or large capacitance values (or both), which require large areas of silicon in order to fabricate on an IC. However, as seen in Figure 10, when the feedback is taken from the parallel input stage **64** where the LO-signal is not present, there is no need for low pass filters in feedback paths, and thus does not require a large area of silicon. (bipolar junction transistors - BJTs - are small and therefore the parallel input stage is small).

Thus what has been shown is a stacked modulator and AGC amplifier, particularly for use in wireless communication devices. The stacked configuration allows the output modulation current to be directly re-used by the AGC amplifier, thereby saving current and hence power. The stacked configuration also avoids an unnecessary signal transformation from current to voltage between the modulator and the AGC amplifier. The stacked configuration is particularly suitable for implementation on an integrated circuit (IC), such as part of a CDMA/GSM dual mode radio. All components can be formed as part of the IC with the possible exceptions of the inductors shown in the various embodiment.

Having described the invention, what is claimed is: